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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/020,872	02/09/98	PLASA G	GR-95-P-1411

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EXAMINER	
LINDSAY JR.W	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 10/04/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/020,872	Plasa
Examiner	**Group Art Unit**
Walter L. Lindsay Jr.	2812

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-10 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-10 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: "the photomask" in line 3 of claim 9 should be "the photoresist mask". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mai et al U.S. Patent No. 4,445,266 in view of Zdebel et al U.S. Patent No. 4,837,176.

Mai disclose a method of a silicon nitride layer that has the properties of being oxidation resistant (col 3 lines 61-64).

Next the length of the channel region of the transistor is defined by a layer of photoresist whereby the gate oxide layer, the polysilicon layer and the silicon nitride layer, not covered by the photoresist are subjected to a plasma etch (col 3 line 65- col 4 line 1).

Next the polysilicon and silicon nitride are used as a mask in an ion implantation step that is performed to implant arsenic ions in a P-type substrate (col 4 lines 10-25).

Since the silicon nitride layer is resistant to oxidation, the oxidation, which is carried out through steam oxidation at 900°C, of the polysilicon layer proceeds laterally and perpendicular to the sidewalls of the polysilicon layer. At the juncture of the lateral edges of the polysilicon layer and the silicon nitride layer, there is a slight uplifting of the silicon nitride layer due to the normal forces incurred in the oxidation process (col 4 lines 61 -68).

Mai does not disclose the formation of a second silicon layer that rest a top the oxidation protection layer thereby forming a second electrode as required by claim 1, nor does Mai disclose forming the oxidation protection layer of oxide-nitride, an oxide-nitride sandwich or an oxide-nitride-oxide sandwich of claims 6,7, and 8 respectively.

Zdebel discloses a method for forming two polysilicon layers, where in between the two layers is a oxidation resistant layer made out of suitable materials, such as silicon nitride or a sandwich of oxide plus nitride (col 7 lines 15-55).

In claim 9 wherein the photomask is in place when the ion implantation takes place is view to be an optimization of this process and would not cause one of ordinary skill in the art undue experimentation to arrive at this step.

In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the steps of placing a second polysilicon layer over the oxidation resistant layer and to have different oxidation materials as stated in Zdebel in the primary invention of Mai to fabricate a conducting structure on a semiconductor substrate to

form a memory cell having a transistor and a capacitor in an integrated circuit, as stated to be prior art by the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay Jr. whose telephone number is (703) 306-5727. The examiner can normally be reached on Monday to Thursday from 7:30 to 5:00.

The examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

WLL
Walter L. Lindsay Jr.
September 27, 1999

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800